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10/562,506	12/23/2005	David Gordon	AAT-106US	7951

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EXAMINER	
UNG, LANNY N	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/562,506	GORDON ET AL.	
	Examiner	Art Unit	
	LANNY UNG	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5, 8-16 and 19-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-16 and 19-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to preliminary amendments filed on March 6, 2006.

Claims 1-5, 8-16 and 19-24 are pending.

Claims 6-7 and 17-18 have been canceled.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 10, 12-13 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by **Ren** (US 2003/0084434).

With respect to **Claim 1**, Ren discloses:

A control device for electrical or electronic equipment, *(digital product, Abstract, line 3)* the device having processing means and non-volatile memory means, *(typical digital product contains a CPU and flash/ROM memory, Paragraph 31, lines 5-7)* the non-volatile memory means having installed programs executable by the processing means directly from the non- volatile memory means, *(a software program resides in Flash/ROM memory and is read by CPU during execution, Paragraph 31, lines 8-10)*

each program being made up of processing elements at least one of which can be modified or upgraded by the Installation of a patch, *(updating software modules in the digital products by use of software patches, Paragraph 11, lines 10-11)*

wherein: a part of the memory means is used as a patch registry containing a list of patch descriptor elements, *(Patch Control Table contains a list of identifiers of the patches that have been programmed into the digital product, Paragraph 47, lines 1-7)*

and the processing means is arranged to install a new patch by modifying the program processing element to which It relates *(CPU is directed to the start address of the software patch and executes the patch, Paragraph 42, lines 2-7)* and storing a patch descriptor element for the patch in the patch registry, *(Patch Control Table contains a list of identifiers of the patches installed, Paragraph 47)* each patch descriptor element containing a list of modified code descriptor elements identifying the processing element to which the patch has been applied. *(Patch Control Table contains a list of corresponding identifiers of the software sections that are updated by the patches, Paragraph 47, lines 1-7)*

With respect to **Claim 2**, all the limitations of **Claim 1** have been addressed above; and Ren further discloses:

A device as claimed in claim 1 in which the patch registry includes information relating to progress of the installation of the new patch. *(Patch Control Table includes information about patches that have been programmed into the digital product (i.e. which patches have completed installation), Paragraph 47, lines 1-5)*

With respect to **Claim 10**, all the limitations of **Claim 1 or 2** have been addressed above; and Ren further discloses:

A device as claimed in claim 1 or 2 in which the modified code descriptor elements include a start address of the memory area used for repaired code contained in the patch. *(patch control routine directs the CPU to jump to the start address of the patch program for updating a particular section of the program, Paragraph 46, lines 12-16)*

With respect to **Claim 12**, Ren discloses:

A method of modifying programs installed in a control device for electrical or electronic equipment, *(digital product, Abstract, line 3)* the control device having processing means and non-volatile memory means, the non-volatile memory means *(typical digital product contains a CPU and flash/ROM memory, Paragraph 31, lines 5-7)* having installed programs executable by the processing means directly from the non-volatile memory means *(a software program resides in Flash/ROM memory and is read by CPU during execution, Paragraph 31, lines 8-10)* and each program being made up of processing elements, *(updating certain program codes in a software section, Paragraph 42, lines 2-4)* the method comprising.

a) downloading to the control device new patch from an external source containing code for modifying one of the program processing elements,

(dispatching/transmitting a software patch from a patch server to one or more digital products, Paragraph 112, lines 1-3)

b) installing the new patch by modifying the one program processing element to which it relates in the non-volatile memory; *(patch data may contain information for updating data area of flash memory, Paragraph 162, lines 1-5; CPU is directed to the start address of the software patch and executes the patch, Paragraph 42, lines 2-7)*

and c) storing a descriptor element for the new patch in a separate part of the non-volatile memory designated as patch registry, *(Patch Control Table contains a list of identifiers of the patches that have been programmed into the digital product, Paragraph 47, lines 1-7)* in which the patch descriptor element is configured to contain a list of modified code descriptor elements identifying the one program processing element to which the new patch has been applied. *(Patch Control Table contains a list of corresponding identifiers of the software sections that are updated by the patches, Paragraph 47, lines 1-7)*

Claims 13 and 21 are method claims corresponding to the device claims above (Claims 2 and 10) and, therefore, are rejected for the same reasons set forth in the rejections of Claims 2 and 10.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-4, 9, 14-15, 20 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ren** (US 2003/0084434) in view of **Peng** (US 2004/0098427).

With respect to **Claim 3**, all the limitations of **Claim 1 or 2** have been addressed above; and Ren does not disclose:

A device as claimed in claim I or 2 in which the patch registry includes a list of unused program memory blocks for each processing element.

However, Peng discloses:

A device as claimed in claim I or 2 in which the patch registry includes a list of unused program memory blocks for each processing element. *(garbage table includes information used to search for unused memory areas of a main program, see Figure 15, Paragraph 106, lines 10-11)*

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Peng into the teaching of Ren to include a patch registry that includes unused program memory blocks for each processing element in order to locate memory blocks of a requested size among the unused one to accommodate new software components. *(Peng, Abstract, lines 1-4 and Paragraph 106, lines 12-16)*

With respect to **Claim 4**, all the limitations of **Claim 3** have been addressed above; and Peng further discloses:

A device as claimed in claim 3 in which, on installation of the new patch, unused program memory in the list is used to extend the patch registry to contain information relating to the new patch. *(if an appropriately sized memory block is found in the unused memory areas, the block is allocated to receive the new EBSC (i.e. patch, updated version), Paragraph 106, lines 17-19)*

With respect to **Claim 9**, all the limitations of **Claim 1 or 2** have been addressed above; and Ren does not disclose:

A device as claimed in claim 1 or 2 in which the modified code descriptor elements identify a number of bytes of faulty code in the processing element being repaired by the patch.

However, Peng discloses:

A device as claimed in claim 1 or 2 in which the modified code descriptor elements identify a number of bytes of faulty code in the processing element being repaired by the patch. *(comparing the size of the new code to the existing code means information on the current size of the original code is known, Paragraph 105, lines 10-12)*

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Peng into the teaching of Ren to include identifying a number of bytes of faulty code being repaired by the patch in order to determine if there is sufficient space for the new patch code in the original location. *(Peng, Paragraph 72, lines 7-19)*

Claims 14-15 and 20 are method claims corresponding to the device claims above (Claims 3-4 and 9) and, therefore, are rejected for the same reasons set forth in the rejections of Claims 3-4 and 9.

With respect to **Claim 23**, all the limitations of **Claim 12 or 13** have been addressed above; and Ren does not disclose:

A method as claimed in claim 12 or 13 in which step (b) comprises overwriting code in the one processing element with code contained in the patch.

However, Peng discloses:

A method as claimed in claim 12 or 13 in which step (b) comprises overwriting code in the one processing element with code contained in the patch. *(when the current location of the original EBSC (processing element) is equal to or less than the new EBSC (patch/update), allocate the original location to receive the new update, Paragraph 105, lines 10-14)*

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Peng into the teaching of Ren to include overwriting the original code with the patch code in order to decrease processing time involved in allocating new memory, erasing and writing data to memory. *(Peng, Paragraph 8, lines 1-15)*

With respect to **Claim 24**, all the limitations of **Claim 12 or 13** have been addressed above; and Ren does not disclose:

A method as claimed in claim 12 or 13 in which step (b) comprises installing the patch code in a selected unused part of the non-volatile memory and diverting program flow to the selected part of the non-volatile memory and back again thereby bypassing code in the unmodified processing element.

However, Peng discloses:

A method as claimed in claim 12 or 13 in which step (b) comprises installing the patch code in a selected unused part of the non-volatile memory *(search for an unused memory area sufficient to store/install the new EBSC, Paragraph 105)* and diverting program flow to the selected part of the non-volatile memory and back again thereby bypassing code in the unmodified processing element. *(update the vector table following the writing of a new version of an EBSC, Paragraph 111, lines 9-12)*

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Peng into the teaching of Ren to include installing patch code in a selected unused part of memory and diverting program flow to the selected part of memory in order to make the correct call to the upgraded/new function instead of the old function. *(Peng, Paragraph 94, lines 11-21)*

Claims 5 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ren** (US 2003/0084434) in view of **Beelitz et al.** (US 6,182,275).

With respect to **Claim 5**, all the limitations of **Claim 1 or 2** have been addressed above; and Ren does not disclose:

A device as claimed in claim 1 or 2 in which each patch descriptor element contains a text description of the patch configured to be presented to a user interface.

However, Beelitz et al. disclose:

A device as claimed in claim 1 or 2 in which each patch descriptor element contains a text description of the patch configured to be presented to a user interface. *(each patch entry contains a description field to appear on the screen of a user interface, Column 10, lines 45-48)*

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Beelitz et al. into the teaching of Ren to include displaying a text description of the patch to a user interface in order to inform the user of the purpose of the patch. *(Bellitz et al., Paragraph 10, lines 47-48)*

Claim 16 is a method claim corresponding to the device claim above (Claim 5) and, therefore, is rejected for the same reasons set forth in the rejection of Claim 5.

Claims 8, 11, 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ren** (US 2003/0084434) in view of **Lillich** (US 5,790,856).

With respect to **Claim 8**, all the limitations of **Claim 1 or 2** have been addressed above; and Ren does not disclose:

A device as claimed in claim 1 or 2 in which the modified code descriptor elements identify a start address of a faulty code block in the processing element.

However, Lillich disclose:

A device as claimed in claim 1 or 2 in which the modified code descriptor elements identify a start address of a faulty code block in the processing element. *(patch library/table contains the original routine pointer which is the address of the given f unction which the particular patch is intended to modify or replace, Column 11, lines 56-59)*

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Lillich into the teaching of Ren to include identifying a start address of a faulty code block in the processing element in order to ensure the correct modules get updated by the correct patches.

With respect to **Claim 11**, all the limitations of **Claim 1 or 2** have been addressed above; and Ren does not disclose:

A device as claimed in claim 1 or 2 in which the modified code descriptor elements contain information in the form of binary flags describing how the repaired code contained in the patch was installed.

However, Lillich disclose:

A device as claimed in claim 1 or 2 in which the modified code descriptor elements contain information in the form of binary flags describing how the repaired code contained in the patch was installed. *(the patch library/table contains a status flag used to indicate whether the particular patch was successfully installed, Column 12, lines 4-5)*

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Lillich into the teaching of Ren to include a binary flag describing how the repaired code contained in the patch was installed in order to indicate to user if/when a particular patch was installed successfully. *(Lillich, Column 12, lines 4-5)*

Claims 19 and 22 are method claims corresponding to the device claims above (Claims 8 and 11) and, therefore, are rejected for the same reasons set forth in the rejections of Claims 8 and 11.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LANNY UNG whose telephone number is (571)270-7708. The examiner can normally be reached on Monday-Thursday, 6:30am-5:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Zhen can be reached on (571)272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/LU/
Lanny Ung
Examiner, Art Unit 2191
February 18, 2010
/Wei Y Zhen/
Supervisory Patent Examiner, Art Unit 2191